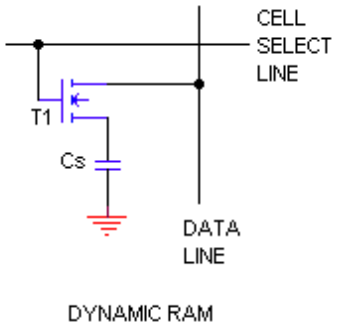
DRAM (Dynamic RAM) Controller

Just like static RAMs, the memory on a dynamic RAM memory chip is organized in a matrix formed by rows and columns of memory cells. The simplest type of dynamic RAM cell contains only one transistor and one capacitor. Whether a 1 or 0 is contained in a cell is determined by whether or not there is a charge on the capacitor. During a read operation, one of the row select lines is brought high by decoding the row address (low-order address bits). The activated row select line turns on the switch transistors for all cells in the selected row. This causes the refresh amplifier associated with each column to sense the voltage level on the corresponding capacitor and interpret it as a 0 or a 1. If it is more than 50 percent, it reads it as a 1; otherwise it reads it as a 0. The column address (high-order address bits) enables one cell in the selected row for the output. The read cycle is actually a read/write cycle. If a '1' is read then the cell is re-written to with a '1' to recharge it. However if a '0' is read no recharge is necessary.



DYNAMIC RAM

During this process, the capacitors in an entire row are disturbed. In order to retain the stored information, the same row of cells is rewritten by the refresh amplifiers. A write operation is done similarly except that the data input is stored in the selected cell while the other cells in the same row are simply refreshed. As a result of the storage discharge through pn-junction leakage current, dynamic memory cells must be repeatedly read and restored, this process is called memory refresh. The storage discharge rate increases as the operating temperature rises, and the necessary time interval between refreshes ranges from 1 to 100 ms.

The capacitor Cs discharges through the internal resistance of the NMOS transistor T1. Typically Cs = 0.2 pF and the internal resistance Rin = 10^{10} ohms, so:

Cs x Rin = $0.2 \times 10^{-12} \times 10^{10} \times 10^{3}$ ms = 2 ms

So the typical refresh time interval is 2 ms. Although a row of cells is refreshed during a read or write, the randomness of memory references cannot guarantee that every word in a memory module is refreshed within the 2-ms time limit. A systematic way of accomplishing a memory refresh is through memory refresh cycles.

Memory Refresh Cycle

In a memory refresh cycle, a row address is sent to the memory chips, and a read operation is performed to refresh the selected row of cells. However, a refresh cycle differs from a regular memory read cycle in the following respects:

1. The address input to the memory chips does not come from the address bus. Instead, the row address is supplied by a binary counter called the refresh address counter. This counter is incremented by one for each memory refresh cycle so that it sequences through all the row

addresses. The column address is not involved because all elements in a row are refreshed simultaneously.

2. During a memory refresh cycle, all memory chips are enabled so that memory refresh is performed on every chip in the memory module simultaneously. This reduces the number of refresh cycles. In a regular read cycle, at most one row of memory chips is enabled.

3. In addition to the chip enable control input, normally a dynamic RAM has a data output enable control. These two control inputs are combined internally so that the data output is forced to its high-impedance mode unless both control inputs are activated. During a memory refresh cycle, the data output enable control is deactivated. This is necessary because all the chips in the same column are selected and their data outputs are tied together. On the other hand, during a regular memory read cycle, only one row of chips is selected, consequently, the data output enable signal to each row is activated.

The memory cells have a whole support infrastructure of other specialized circuits. These circuits perform functions such as:

* Identifying each row and column (row address select and column address select)
* Keeping track of the refresh sequence (counter)
* Reading and restoring the signal from a cell (sense amplifier)
* Telling a cell whether it should take a charge or not (write enable)

Other functions of the memory controller include a series of tasks that include identifying the type, speed and amount of memory and checking for errors.

Memory Refresh Period

Consider a memory module of 16K bytes implemented by 4K x I dynamic RAMs. Each chip has 64 rows and 64 columns of memory cells and has separate row address (6 bits) and column address (6 bits) pins. The memory refresh cycle signal, which indicates that a refresh is in progress, can be generated by a refresh cycle timing generator in the memory module. If the current cycle is a refresh cycle, the 2-to-1 multiplexer selects the row address from the refresh address counter, otherwise the row address comes from the address bus. Assuming that every cell in the chip array must be refreshed within a 2-ms time interval, a refresh cycle is required for every $(2 \times 10^{-3}/64)$ = 31.25 µs. At the end of each refresh cycle, the binary counter is incremented by 1 so that it points to the next row to be refreshed. During a refresh cycle, all chips on the module are enabled for performing a read operation by activating the chip enable signals. Their data outputs are forced into the high-impedance state by deactivating the output enable signals.

In addition to requiring refresh logic, a disadvantage in using dynamic RAMs is that during a refresh cycle the memory module cannot initiate a read or write cycle until the refresh cycle has been completed. As a result, a read or write request will take up to twice as long to complete if a refresh is in progress. Assuming a cycle time of 400 ns :

$$\frac{(64 \times 400 \times 10^{-9})}{(2 \times 10^{-3})} \times 100\% = 1.28\%$$

1.28% of the memory time is spent on refresh.